**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (currently amended): An apparatus ~~for a compression architecture utilizing internal cache residing in main memory, the main memory~~ comprising:

a main memory including:

a compression cache to store a plurality of uncompressed data, wherein the compression cache is organized as a sectored cache that has associated tags that are on-die, wherein a tag match is performed between a memory access request and the associated tags and a hit signal is sent to a memory controller coupled to the main memory to schedule an uncompressed data access from the compression cache if a hit occurs;

a compressed memory to store a plurality of compressed data; and

a compressed memory pointer table (CMPT) to store a plurality of pointers, the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations.

Claim 2 (canceled)

Claim 3 (original): The apparatus of claim 1 wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus.

Claim 4 (original): The apparatus of claim 1 wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.

Claim 5 (currently amended): The apparatus of claim 3, wherein the ~~apparatus is coupled to the~~ memory interface ~~that~~ comprises:

a victim buffer to store at least one entry that has been evicted from the compression cache;

a CMPT offset calculator to provide an offset relative to the start of the CMPT based on an actual address of ~~the~~ data ~~being~~ to be compressed and stored in the cache memory.

Claim 6 (original): The apparatus of claim 5 wherein the memory interface is incorporated within a processor or a chipset.

Claim 7 (original): The apparatus of claim 6 wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset.

Claim 8 (currently amended): The apparatus of claim 5 wherein the entry is to be evicted based on a first in first out (FIFO) protocol.

Claim 9 (previously presented): The apparatus of claim 1 wherein the CMPT is to store the plurality of pointers to the plurality of compressed data sequentially based on memory addresses for the plurality of compressed data.

Claim 10 (currently amended): An apparatus for a memory interface comprising:

the memory interface including:

a first cache to store a plurality of tags for a compression cache of a main memory coupled to the memory interface, the compression cache to store a plurality of uncompressed data;

a victim buffer to store at least one entry that has been evicted from the compression cache and to directly supply the at least one entry to a requester if a tag match occurs in the victim buffer;

an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) of the main memory that is to store pointers to compressed data stored in a compressed memory of the main memory, based on an actual address of a data being compressed; and

a second cache to store a plurality of pointers for the CMPT, the apparatus to assign a higher priority to compressed memory read operations in comparison to other operations.

Claim 11 (original): The apparatus of claim 10 wherein the memory interface is incorporated within a processor or a chipset.

Claim 12 (original): The apparatus of claim 11 wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset.

Claim 13 (original): The apparatus of claim 10 wherein the entry is evicted based on a first in first out (FIFO) protocol.

Claim 14 (currently amended): A method comprising:

receiving a memory address for a memory operation;

storing a plurality of compressed data in a compressed memory in a main memory; ~~and~~

performing a tag match between the memory address and a first cache of a memory interface coupled to the main memory storing a plurality of tags for a ~~compressed memory~~ compression cache in the main memory; and ~~, assigning a higher priority to compressed memory read operations in comparison to other operations~~

accessing a plurality of uncompressed data from the compression cache responsive to an uncompressed access scheduling by a memory controller if the tag match resulted in a hit, and if the tag match resulted in a miss, accessing the plurality of uncompressed data directly from a victim buffer of the memory interface if the plurality of uncompressed data is present in the victim buffer.

Claim 15 (cancel)

Claim 16 (original): The method of claim 14 further comprising locating a pointer and subsequently finding a compressed memory location based at least in part on the pointer if the tag match resulted in a miss for the memory operation for a read miss.

Claim 17 (original): The method of claim 14 further comprising compressing the data and storing it in a compressed memory location for the memory operation for a write miss.

Claim 18 (currently amended): A system comprising:

a processor; and

a main memory, coupled to the processor, with:

a compression cache to store a plurality of uncompressed data, wherein the compression cache is organized as a sectored cache that has associated tags that are on-die, wherein a tag match is performed between a memory access request and the associated tags and a hit signal is sent to a memory controller coupled to the main memory to schedule an uncompressed data access from the compression cache if a hit occurs;

a compressed memory to store a plurality of compressed data; and

a compressed memory pointer table (CMPT) to store a plurality of pointers, and to assign a higher priority to compressed memory read operations in comparison to other operations.

Claim 19 (original): The system of claim 18 wherein the compression cache is a sectored cache.

Claim 20 (previously presented): The system of claim 18 wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface.

Claim 21 (previously presented): The system of claim 18 wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.

Claim 22 (currently amended): A system comprising:

a processor; and

a memory interface, coupled to the processor, with:

a first cache to store a plurality of tags for a compression cache of a main memory coupled to the memory interface, the compression cache to store a plurality of uncompressed data;

a memory controller to schedule an uncompressed data access from the compression cache if a tag match operation between the plurality of tags and an access request results in a hit;

a victim buffer to store at least one entry that has been evicted from the compression cache;

an offset calculator to provide an offset relative to the start of a Compressed Memory Pointer Table (CMPT) of the main memory that is to store pointers to compressed data stored in a compressed memory of the main memory, based on an actual address of a data being compressed; and

a second cache to store a plurality of most recently used pointers for the CMPT.

Claim 23 (original): The system of claim 22 wherein the memory interface is incorporated within a processor or a chipset.

Claim 24 (canceled)

Claim 25 (original): The system of claim 22 wherein the entry is evicted based on a first in first out (FIFO) protocol.

Claim 26 (currently amended): A system comprising:

a processor, coupled to a memory bridge, the memory bridge to comprise;

a first cache to store a plurality of tags for a compression cache of a main memory coupled to the memory bridge, the first cache to perform a tag match operation between the plurality of tags and an incoming memory address;

a victim buffer to store at least one entry that has been evicted from the compression cache;

a memory controller to schedule an uncompressed data access from the compression cache if the tag match operation results in a hit;

an offset calculator to provide an offset relative to the start of a Compressed Memory Pointer Table (CMPT) of the main memory that is to store pointers to compressed data stored in a compressed memory of the main memory, based on an actual address of a data that is compressed; and

a second cache to store a plurality of pointers for the CMPT address; and

[[a]] the main memory, coupled to the memory bridge, to comprise;

[[a]] the compression cache to store a plurality of uncompressed data;

a compressed memory to store a plurality of compressed data; and

a compressed memory pointer table (CMPT) to store a plurality of pointers.

Claim 27 (original): The system of claim 26 wherein the compression cache is a sectored cache.

Claim 28 (previously presented): The system of claim 26 wherein the compression cache has a plurality of associated tags that are incorporated within the memory bridge.

Claim 29 (original): The system of claim 26 wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.